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AS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/247,413	02/10/99	LO	Y NOR-9

020808
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IM22/0627

EXAMINER	
ANDERSON, M	
ART UNIT	PAPER NUMBER
1765	8

DATE MAILED: 06/27/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/247,413	Lo et al.
Examiner	**Group Art Unit**
Matt Anderson	1765

☒ Responsive to communication(s) filed on *4/17/00*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-12 and 14-20* is/are pending in the applicat

Of the above, claim(s) *14-17* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-12* is/are rejected.

☒ Claim(s) *18-20* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I in Paper No. 7 is acknowledged.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-4,7-8, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. in view of Lee et al. (US 4,900,372) and Narayan et al. (US 5,208,182).

Shimbo et al. discloses the bonding of InP and GaP single crystal substrates in Figs. 2A and 2B. In Col. 1 lines 48-61, the known need for lattice constant match between the layer grown and the substrate during epitaxy is described. Lattice mismatch between layers is described as an important processing parameter. GaAs and AlGaAs are described as capable of forming a good heterojunction epitaxially. In Col. 3 lines 6-38 is described the process of

Shimbo et al. The bonded substrates are annealed at between 200-600'C with the exact temperature depending on the substances being bonded. In lines 23-29 the thermal expansion mismatch of bonded substrates is described as preferably below 2 x 10^{-6}/'C. Otherwise mechanical failure (i.e. cracking) occurs at the boundary. The thermal expansion of bonded substrates is an important processing parameter. The bonded substrates described are GaAs/InP, ZnS/GaAs, InP/InSb, GaP/InP, CdS/InP, GaAs/ GaAs, InP/InP. In Example 4, a substrate of thickness 60 μm was bonded to a second substrate of

Shimbo et al. does not describe the so formed device as a substrate for further fabrication.

Lee et al. discloses in the abstract a method of annealing deposited layers of III-V compound semiconductors when deposited on Si, Ge/Si, or other single crystal substrates. In Col. 3 lines 42+ is described the formation of thermal strain layers and buffer layer)s and their anneal cycle. Lee et al. in Col. 4 lines 1-17 describe typical buffer layers as GaAs, InGaAs, and AlGaAs. The second buffer layer is described as also annealed. One of ordinary skill in the art would recognize the anneal steps as for the purpose of reducing the crystal imperfections in the buffer layers. Described in col. 4 lines 5-21 is the need to optimize conditions depending on the material used.

Narayan et al. discloses the formation of a super lattice buffer layer and the repeating of the superlattice buffer layers until the buffer layer is greater than the critical thickness for bending the dislocations. In Col. 6 lines 3+, the method is described in more detail.

It would have been obvious to combine the references of Shimbo et al., Lee et al., and Narayan because Shimbo et al. produces a construct which would be useful as a substrate and Lee et al. and Narayan disclose the formation of buffer layers on substrates of the same materials as the substrates of Shimbo et al. and because such a combination would have been anticipated to produce an expected result.

In regard to claim 1, it would have been obvious to one of ordinary skill in the art to form a bonded substrate from GaP, InP and to choose layers to be subsequently formed on that substrate to have compatible thermal expansion properties and lattice constant properties because the prior art recognizes that the these parameters need to be optimized according to the material used and these materials were known. The mental steps of 'choosing' and 'determining' according to the known materially inherent process parameters of lattice constant mismatch and thermal constant mismatch are essentially claims for optimizing these known process parameters and would have been anticipated to produce an expected result.

In regard to claim 2-4, it would have been obvious to one of ordinary skill in the art at the time of the present invention to grow a buffer layer on either face of the substrate because Lee discloses the formation of a buffer layer on a single crystal substrate (of which, a InP/GaP bonded substrate is one) and because such a combination would have been anticipated to produce an expected result.

In regard to claim 2, It would have been obvious to one of ordinary skill in the art at the time of the present invention to repeat the growing and annealing of the substrate because

Narayan et al. discloses such buffer layer constructs that are added to until the critical dislocation bending thickness is reached and such a process would have been anticipated to produce an expected result.

4. Claims 5-6, 9-11,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. and Lee et al. and Narayan eta l. as applied to claim s 1-4,7-8 above, and further in view of Furuyama et al. (US 4,992,386).

Shimbo et al. discloses the bonding of InP and GaP substrates as described above.

Shimbo et al. does not describe further device fabrication.

Lee et al. discloses a method of annealing deposited layers of III-V compound semiconductors when single crystal substrates as described above..

Lee does not disclose further device fabrication after the buffer layer.

Narayan et al. discloses the formation of a buffer layer of critical thickness to bend dislocations as described above.

Furuyama et al. discloses a semiconductor device as is seen in Fig. 5. InP has GaInAs deposited thereon. InP is seen to be deposited thereon with a further deposition of InP (an InP based semiconductor).

It would have been obvious to one of the ordinary skill in the art at the time of the present invention to combine the references because all dealt with III-V semiconductors and the lattice

engineering of the inherent thermal and lattice properties of the materials thereof and because such a combination would have been anticipated to produce an expected result.

In regard to claims 5-6, 11, 12 , it would have been obvious to grow a first epilayer (InP) on a buffer layer (GaInAs intermediate buffer layer) and a second epilayer (InP) on the first epilayer because such a growth sequence was suggested in the art (Furuyama et al.) and because such a growth sequence would have been anticipated to produce an expected result.

In regard to claims 9 and 10, 12, it would have been obvious at the time of the present invention to one of ordinary skill in the art to form the buffer layer from AlGaAs, or InGaAs and the first and second epilayers from InP because such materials are suggested by the combined references and because such a use of these materials would have been anticipated to produce an expected result.

In regard to claim 12, the mental steps of 'choosing', 'determining', 'ensuring' according to the known materially inherent process parameters of lattice constant mismatch and thermal constant mismatch are essentially claims for optimizing these known process parameters and would have been anticipated to produce an expected result.

Allowable Subject Matter

5. Claims 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The ratio of the thicknesses of the bonded substrates has not been discussed as an important process parameter in the prior art.

Response to Arguments

7. Applicant's arguments with respect to claim have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Anderson whose telephone number is (703) 308-0086. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Benjamin Utech, can be reached at (703) 308-3836.

Any inquiry of a general nature can be directed to the group receptionist whose telephone number is (703) 308-0661.

MAA

June 26, 2000

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